Attorney Docket No.: A0312.70521US00
Express Mail Label No.: EV 292 459 643 US
Date of Deposit: February 25, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Brian David Johansson et al.
Serial No:	Not Yet Assigned
Confirmation No:	Not Yet Assigned
Filed:	Herewith
For:	LOGIC LEVEL VOLTAGE TRANSLATOR
Examiner:	Not Yet Assigned
Art Unit:	Not Yet Assigned

MAIL STOP: PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 CFR §§1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§1.56, 1.97 and 1.98, the Applicant requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. §1.97

This Information Disclosure Statement has been filed before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. §1.114.

No fee or certification is required.

PART II: Information Cited

The Applicant hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified). The order of presentation of the references should not be construed as an indication of the importance of the references.

PART III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 be signed by the Examiner to evidence that the cited information has been fully considered by the Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the Applicant makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, the Applicant makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56(b).

By submitting this Information Disclosure Statement, the Applicant makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. §102.

Notwithstanding any statements by the Applicant, the Examiner is urged to form his own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

Respectfully submitted,
Brian David Johansson et al., Applicant(s)

By: _____

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FORM PTO-1449/A and B (Modified)	APPLICATION NO.: Not Yet Assigned	ATTY. DOCKET NO.: A0312.70521US00
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE: Herewith	CONFIRMATION NO.: Not Yet Assigned
	APPLICANT: Brian D. Johannson et al.	
Sheet 1 of 1	GROUP ART UNIT: Not Yet Assigned	EXAMINER: Not Yet Assigned

U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or of issue of Cited Document MM-DD-YYYY
		Number	Kind Code		
	A1	6,650,168	B1	Wang et al.	11/18/2003
	A2	6,556,061	B1	Chen et al.	04/29/2003
	A3	6,489,828	B1	Wang et al.	12/03/2002
	A4	6,414,534	B1	Wang et al.	07/02/2002

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document (not necessary)	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/ Country	Number	Kind Code			

OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)	
	C1	Wen-Tai Wang et al., "Level Shifters for High-Speed 1-V to 3.3 V Interfaces in a 0/13-μm Cu-Interconnection/Low-k CMOS Technology; pp. 307-310, 2001 IEEE;		
	C2	Texas Instruments Translation Overview; pp. 1-4, 2003;		
	C3	"Voltage Level Translating Circuit", Oct. 1959, IBM Technical Disclosure Bulletin;		
	C4	"Voltage Level Translation Circuit:, June 1975, pp. 1-2, IBM Technical Disclosure Bulletin;		
	C5	Charles D. Rakes, "Circuit Circus", pp. 59-62; March 1999, Popular Electronics;		
	C6	"Cascaded Common-Gate FET IC Provides Flexible Level Translation:, Electronic Design, pp. 1 of 5; 2/3/04		

EXAMINER	DATE CONSIDERED